AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) An image processing apparatus comprising:

a pixel matrix formation section having a rewritable circuit configuration, and having a plurality of line memories that form a pixel matrix based on pixel data and output the pixel data in parallel;

a filtering circuit having a rewritable circuit configuration, and performing filtering of pixel data by use of **[[a]]** the pixel matrix based on the pixel data received in parallel from the line memories;

a memory for storing setting information for rewriting the circuit configurations of the pixel matrix formation section and the filtering circuit; and

a controller for rewriting a configuration of the line memories and the circuit configuration of the filtering circuit by use of the setting information stored in the memory based on an image processing condition.

2. (Previously Presented) An image processing apparatus as claimed in Claim 1, wherein said image processing condition is an output image size.

3. (Previously Presented) An image processing apparatus as claimed in Claim 1, wherein said image processing condition is a processing speed.

4. (Original) An image processing apparatus as claimed in Claim 1, further comprising:

an operation panel for setting the image processing condition.

5. (Previously Presented) An image processing apparatus as claimed in Claim 4, wherein said controller rewrites the circuit configuration in accordance with an operation mode set with the operation panel.

6. (Original) An image processing apparatus as claimed in Claim 1, wherein said filtering circuit is used for image area determination.

7. (Original) An image processing apparatus as claimed in Claim 6, wherein the filtering circuit performs filtering for detecting an isolated point of an image.

8. (Currently Amended) An image processing apparatus comprising:

a processing circuit having a plurality of line memories that form a pixel matrix based on pixel data and performing filtering of the pixel data by use of **[[a]]** the pixel matrix ~~based on pixel data~~ from the line memories;

a memory for storing setting information for rewriting a configuration of the processing circuit; and

a controller for rewriting a configuration of the line memories of the processing circuit and the configuration of filtering by use of the setting information stored in the memory based on an image processing condition.

9. (Previously Presented) An image processing apparatus as claimed in Claim 8, wherein said image processing condition is an output image size.

10. (Previously Presented) An image processing apparatus as claimed in Claim 8, wherein said image processing condition is a processing speed.

11. (Original) An image processing apparatus as claimed in Claim 8, further comprising:

an operation panel for setting the image processing condition.

12. (Previously Presented) An image processing apparatus as claimed in Claim 11, wherein said controller rewrites the configuration of the processing circuit in accordance with an operation mode set with the operation panel.

13. (Original) An image processing apparatus as claimed in Claim 8, wherein said processing circuit is used for image area determination.

14. (Original) An image processing apparatus as claimed in Claim 13, wherein the processing circuit performs filtering for detecting an isolated point of an image.

15. (Canceled)

16. (Previously Presented) An image processing apparatus as claimed in Claim 1, wherein the image processing condition is selectable from multiple values for a given output device.

17. (Previously Presented) An image processing apparatus as claimed in Claim 8, wherein the image processing condition is selectable from multiple values for a given output device.

18. (Canceled)